Design and development of Rapid Prototype board for FADEC Engine controller validation

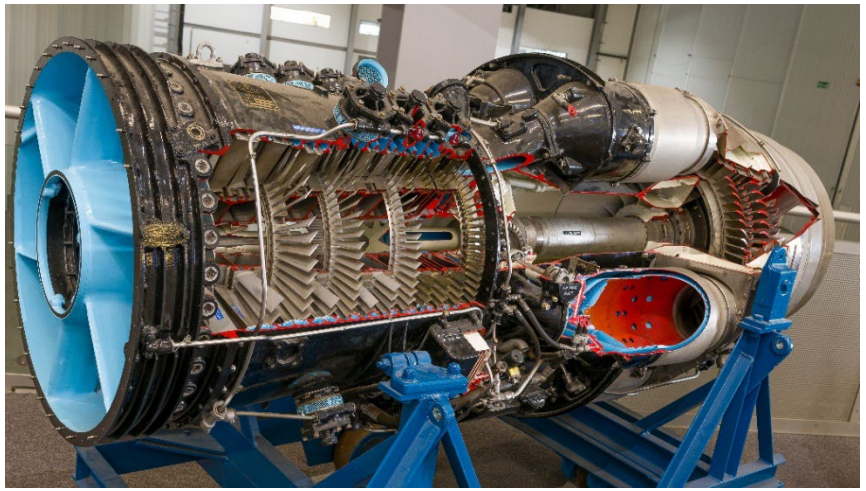
Indian Aerospace Manufacturer

Summary

- Rapid control Prototype for an Aero Engine Controller (FADEC)
- Developed to test the control algorithm of aero engines
- Dual Redundant Architecture
- Algorithm implemented inside Cyclone IV FPGA from Altera
- Hardware based multitasking, less load on software
- Modular Design

Scope

- Hardware Development
  - Requirement Analysis
  - Hardware Design
  - Schematic Capture
  - PCB Design
  - PCB Fabrication and Assembly
- Support for control algorithm development
- Wiring Harness Preparation
- Mechanical Casing Development
- System Testing



Challenges/ Highlights

Signal processing and Interfacing solutions for LVDT, RVDT, RTD, Thermocouple, Pressure sensor, voltage inputs, current inputs, stepper-motors, ARINC, RS485, etc.

Tools & Standards

- ANSYS SCADE
- IBM RTRT

Standard: DO- 178 C